Receipt

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Suraj J. Mathew et al.

Title: METHOD TO FABRICATE SURFACE P-CHANNEL CMOS

Docket No.: 303.744US1
Filed: March 14, 2001
Examiner: Unknown

Serial No.: 09/808,261
Due Date: N/A
Group Art Unit: 2812

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the attached:

X Communication Re: Incorrect Filing Receipt (1 pg.)

X Copy of Filing Receipt (1 pg.)

X A return postcard.

X Copy of First page of the Application (1 pg.)

No Additional fee is required.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By:
Name: David C. Peterson
Reg. No. 47,857
DCP:CMG:clh

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 9 day of May, 2001.

Chris Hammond
Name

Chris Hammond
Signature

S/N 09/808,261

PATENT

#2/CR
9/13/01
V. Vannucci

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.:	09/808,261	Group Art Unit:	2812
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COMMUNICATION RE: INCORRECT FILING RECEIPT

Commissioner for Patents
Washington, D.C. 20231

Applicants hereby request correction of the Filing Receipt with respect to the above-identified patent application. In the Filing Receipt received May 3, 2001, (copy enclosed), the Title is incorrect. The Filing Receipt reads: **Method to Fabricate Surface P-Channel Transistor CMOS**. The Filing Receipt should read: **Method to Fabricate Surface P-Channel CMOS**. This is evidenced by the first page of the application (copy enclosed).

Applicants would appreciate the above-identified printing error be corrected and that a new "corrected" filing receipt be sent to Applicants' representatives at the address given below.

Respectfully submitted,

SURAJ J. MATHEW ET AL.

By their Representatives,

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Date 5/7/01 By

David C. Peterson
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Chris Hammond
Chris Hammond

UNITED STATES PATENT AND TRADEMARK OFFICE

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WASHINGTON, D.C. 20231
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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/808,261	03/14/2001	2812	1730	303.744US1	7	50	9

CONFIRMATION NO. 3364

FILING RECEIPT

OC000000006006392

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: David C. Peterson
P.O. Box 2938
Minneapolis, MN 55402

Date Mailed: 04/25/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

DJ 14 JUNE 2001 - 3 MO. 1 DF
14 JAN. 2002 - 10 MO. FF
14 MAR. 2002 - CONV. EXP.

Applicant(s)

Suraj J. Mathew, Boise, ID;
Jigish D. Trivedi, Boise, ID;

Assignment For Published Patent Application

Micron Technology, Inc.;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted 04/24/2001

Projected Publication Date: 09/19/2002

Non-Publication Request: No

Early Publication Request: No

Title

Method to fabricate surface p-channel transistor CMOS

METHOD TO FABRICATE SURFACE P-CHANNEL CMOS

Field of the Invention

The invention relates to the fabrication of semiconductor devices, such as dynamic random access memory devices, and more particularly to patterning and fabrication surface p-channel transistor devices.

Background of the Invention

Complementary metal-oxide-semiconductor (CMOS) technology is widely used in integrated circuits (ICs) due to the lower power consumption as compared to previously preferred NMOS or Bipolar IC's. CMOS is so named because it uses both p- and n-channel transistors in its ICs. However, fabricating both p-channel and n-channel transistors on the same IC adds a number of processing steps to the IC fabrication process.

The n-channel devices typically require n+ poly silicon gate material to set the correct turn-on voltage (threshold). The p-channel devices can be either a buried channel or surface channel device depending on whether n+ or p+ poly silicon is used for the gate material. When a p-channel transistor uses the same n+ poly silicon material as the NMOS device, then it is considered to be a buried p-channel device and the subsequent fabrication process becomes cost-effective. As a result, buried p-channel devices were predominantly used in DRAM and SRAM technologies. The disadvantage of buried p-channel devices is that they are slow (lower current drive) and have non-scalable threshold voltages. DRAM's, till recently, decided to stay with the buried p-channel transistors since it kept the rest of the processing in the array and peripheral n-channel transistors simpler. On the other hand, to achieve higher speed and voltage scalability the SRAM's elected to switch to surface p-channel devices. CMOS with surface p-channel transistors, however, needed a hardened gate oxide and two separate formations of gate poly silicon (n+ and p+) resulting in an extra masking step. With the addition of across

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CONFIRMATION NO. 3364

Bib Data Sheet

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/808,261	03/14/2001 RULE	438	2812	303.744US1

APPLICANTS

Suraj J. Mathew, Boise, ID;
Jigish D. Trivedi, Boise, ID;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 04/24/2001

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no	ID	7	50	9
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged _____ Examiner's Signature _____ Initials				

ADDRESS

Schwegman, Lundberg, Woessner & Kluth, P.A.
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Minneapolis , MN 55402

TITLE

Method to fabricate surface p-channel CMOS

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1730	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit